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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,302	03/04/2002	Shigenari Kotaka	NEC N01321	6641

7590 05/18/2005

Norman P. Soloway
HAYES SOLOWAY P.C.
130 W. Cushing Street
Tucson, AZ 85701

EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,302	KOTAKA, SHIGENARI	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Applicant's request for reconsideration filed on 1/28/2005 has been reviewed.

2. The amendment filed on 1/28/2005 has been entered (including amended claims).

3. The applicant's arguments and the Idea Proposal filed on 11/20/2000 have been considered but are insufficient to overcome the Ishiwaki (US 6,725,415 B2) reference. The Declaration under 37 CFR 1.131 is missing.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 13-18 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims 13-18 consist solely of mathematical operations and solve a purely mathematical problem.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 13, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiwaki (US 6,725,415 B2) in view of Hyodo et al. (US 5,282,215).

As per claim 13, Ishiwaki teaches an arithmetic operation method for a cyclic redundancy check, which performs arithmetic operations for error detection on data to be transmitted (col. 1, lines 8-11, Ishiwaki) using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished (col. 3, lines 49-50, Ishiwaki).

However Ishiwaki does not explicitly teach the specific use of adding a result from each of said arithmetic operations to said data, said arithmetic operation method comprising: first arithmetic operation processing in which a first arithmetic operation is performed on said data by a specified number of bits using a first generative polynomial; second arithmetic operation processing in which a second arithmetic operation is performed on said data by a specified number of bits using at least one piece of a second generative polynomial being same as or different from said first generative polynomial; and third arithmetic operation processing in which a third arithmetic operation is performed on said data of a specified number of bits and on at least one piece of an arithmetic operation result being obtained at a midpoint in either of said first arithmetic operation or said second arithmetic operation, or in both said first arithmetic operation and second arithmetic operation.

Hyodo et al. in an analogous art teach that a continuous CRC arithmetic unit is comprised of: a first CRC arithmetic unit, operatively connected to said shift register, to divide the delayed bit train by a generator polynomial used for the CRC operation and output a remainder obtained as a first CRC arithmetic operation result; a second CRC arithmetic unit, operatively connected to receive the input bit train, to divide the input bit train by the generator polynomial and output a remainder obtained as a second CRC arithmetic operation result; and a subtraction unit, operatively connected to said first and second CRC arithmetic units and said synchronization control unit, to obtain a difference between the first CRC arithmetic operation result and the second CRC arithmetic operation result to produce the current CRC arithmetic operation result in a time series manner for said synchronization control unit (col. 28, lines 13-32, Hyodo et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ishiwaki's patent with the teachings of Hyodo et al. by including an additional step of adding a result from each of said arithmetic operations to said data, said arithmetic operation method

comprising: first arithmetic operation processing in which a first arithmetic operation is performed on said data by a specified number of bits using a first generative polynomial; second arithmetic operation processing in which a second arithmetic operation is performed on said data by a specified number of bits using at least one piece of a second generative polynomial being same as or different from said first generative polynomial; and third arithmetic operation processing in which a third arithmetic operation is performed on said data of a specified number of bits and on at least one piece of an arithmetic operation result being obtained at a midpoint in either of said first arithmetic operation or said second arithmetic operation, or in both said first arithmetic operation and second arithmetic operation.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to simultaneously process a plurality of bits in a clock cycle to perform a CRC operation at a high speed.

- As per claim 19, Ishiwaki and Hyodo et al. teach the additional limitations.

Ishiwaki teaches an arithmetic operation circuit for a cyclic redundancy check, which performs arithmetic operations for error detection on data to be transmitted (col. 1, lines 8-11, Ishiwaki) using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished (col. 3, lines 49-50, Ishiwaki).

Hyodo et al. teach adding a result from each of said arithmetic operations to said data, said arithmetic operation circuit comprising: a first arithmetic operation section to perform a first arithmetic operation on said data by a specified number of bits using a first generative polynomial; a second arithmetic operation section to perform a second arithmetic operation on said data by said specified number of bits using at least one piece of a second generative polynomial being same as or different from said first generative polynomial; and a third arithmetic operation section to perform a third arithmetic operation on said data of said specified number of bits and on at least one piece of an arithmetic operation result being obtained at a midpoint in either of said first arithmetic operation or said second arithmetic operation, or in both said first arithmetic operation and said second arithmetic operation using at least one piece of said second generative polynomial (col. 28, lines 13-32, Hyodo et al.).

8. Claims 14, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiwaki (US 6,725,415 B2) and Hyodo et al. (US 5,282,215) as applied to claim 13 above, and further in view of Henriksen (US 6,324,670 B1).

As per claim 14, Ishiwaki and Hyodo et al. substantially teach the claimed invention described in claim 13 (as rejected above).

However Ishiwaki and Hyodo et al. do not explicitly teach specifically that in the third arithmetic operation processing, the third arithmetic operation is performed by handling the data of the specified number of bits as low-order bits and by handling at least one piece of the third arithmetic operation result as high-order bits.

Henriksen in an analogous art teaches that the low and high order bit portions 408a, 408b are each 16-bits (figure 4, col. 6, lines 14-15, Henriksen).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ishiwaki's patent with the teachings of Henriksen by including additionally that in the third arithmetic operation processing, the third arithmetic operation is performed by handling the data of the specified number of bits as low-order bits and by handling at least one piece of the third arithmetic operation result as high-order bits.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to simplify the circuit design for arithmetic processing of the bits for faster and accurate processing of the data.

- As per claim 20, Ishiwaki and Hyodo et al. and Henriksen teach the additional limitations.

Henriksen teaches a data combining section to combine the data of said specified number of bits handled as low-order bits with at least one piece of said arithmetic operation result handled as high-order bits and to feed combined results to said third arithmetic operation section (figure 4, col. 6, lines 14-15, Henriksen).

9. Claims 15, 17, 21, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiwaki (US 6,725,415 B2) in view of Hyodo et al. (US 5,282,215) and Douady et al. (US 6,516,004 B1).

As per claim 15, Ishiwaki teaches an arithmetic operation method for a cyclic redundancy check, which performs arithmetic operations for error detection on data to be transmitted (col. 1, lines 8-11, Ishiwaki) using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished (col. 3, lines 49-50, Ishiwaki).

However Ishiwaki does not explicitly teach the specific use of adding a result from each of said arithmetic operations to said data, said arithmetic operation method comprising: first arithmetic operation processing in which a first arithmetic operation is performed on said data by 32 bits using a generative polynomial; second arithmetic operation processing in which a second arithmetic operation is performed on said data using a generative polynomial; and third arithmetic operation processing in which a third arithmetic operation is performed on said data of 32 bits and on the first arithmetic operation result of 32 bits being obtained at a midpoint in said first arithmetic operation processing using said generative polynomial.

Hyodo et al. in an analogous art teach that a continuous CRC arithmetic unit is comprised of: a first CRC arithmetic unit, operatively connected to said shift register, to divide the delayed bit train by a generator polynomial used for the CRC operation and output a remainder obtained as a first CRC arithmetic operation result; a second CRC arithmetic unit, operatively connected to receive the input bit train, to divide the input bit train by the generator polynomial and output a remainder obtained as a second CRC arithmetic operation result; and a subtraction unit, operatively connected to said first and second CRC arithmetic units and said synchronization control unit, to obtain a difference between the first CRC arithmetic operation result and the second CRC arithmetic operation result to produce the current CRC arithmetic operation result in a time series manner for said synchronization control unit (col. 28, lines 13-32, Hyodo et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ishiwaki's patent with the teachings of Hyodo et al. by including an additional step of adding a result from each of said arithmetic operations to said data, said arithmetic operation method comprising: first arithmetic operation processing in which a first arithmetic operation is performed on said data by 32 bits using a generative polynomial; second arithmetic operation processing in which a second arithmetic operation is performed on said data using a generative polynomial; and third arithmetic

operation processing in which a third arithmetic operation is performed on said data of 32 bits and on the first arithmetic operation result of 32 bits being obtained at a midpoint in said first arithmetic operation processing using said generative polynomial.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to simultaneously process a plurality of bits in a clock cycle to perform a CRC operation at a high speed.

Ishiwaki also does not explicitly teach the specific use of a thirty-second order generative polynomial; and a sixteenth order generative polynomial.

However Douady et al. in an analogous art teach the error checking code, comprised either of a sequence of 16 binary elements obtained from a generating polynomial x.sup.16 +x.sup.12 +x.sup.5 +1, or by a sequence of 32 binary elements obtained from a generating polynomial x.sup.32 +x.sup.26 +x.sup.23 +x.sup.22 +x.sup.16 +x.sup.12 +x.sup.11 +x.sup.10 +x.sup.8 +x.sup.7 +x.sup.5 +x.sup.4 +x.sup.2 +x+1 (col. 1, lines 59-64, Douady et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ishiwaki's patent with the teachings of Douady et al. by including an additional step of using a thirty-second order generative polynomial; and a sixteenth order generative polynomial.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a thirty-second order generative polynomial; and a sixteenth order generative polynomial would provide the opportunity to generate the CRC from the information bits and the generative polynomial and the CRC is used for detecting a data transmission error.

- As per claim 17, Ishiwaki, Hyodo et al. and Douady et al. teach the additional limitations.

Ishiwaki teaches an arithmetic operation method for a cyclic redundancy check which performs arithmetic operations for error detection on data to be transmitted (col. 1, lines 8-11, Ishiwaki) using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished (col. 3, lines 49-50, Ishiwaki).

Hyodo et al. teach adding a result from each of said arithmetic operations to said data, said arithmetic operation method comprising: first arithmetic operation processing in which a first arithmetic operation is performed on said data by 32 bits using a generative polynomial; second arithmetic operation processing in which a second arithmetic operation is performed on said data by 32 bits using said generative polynomial; third arithmetic operation processing in which a third arithmetic operation is performed on said data of 32 bits and on a first arithmetic operation result of 16 bits being obtained at a midpoint in said first arithmetic operation processing using said generative polynomial; fourth arithmetic operation processing in which a fourth arithmetic operation is performed on said data by 32 bits using said generative polynomial; and fifth arithmetic operation processing in which a fifth arithmetic operation is performed on said data of 32 bits, said first arithmetic operation result of 16 bits, and a second arithmetic operation result of 16 bits being obtained at a midpoint in said second arithmetic operation processing using said generative polynomial (col. 28, lines 13-32, Hyodo et al.).

Douady et al. teach a sixteenth order generative polynomial (col. 1, lines 59-61, Douady et al.).

- As per claim 21, Ishiwaki, Hyodo et al. and Douady et al. teach the additional limitations.

Ishiwaki teaches an arithmetic operation circuit for a cyclic redundancy check, which performs arithmetic operations for error detection on data to be transmitted (col. 1, lines 8-11, Ishiwaki) using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished (col. 3, lines 49-50, Ishiwaki).

Hyodo et al. teach adding a result from each of said arithmetic operations to said data, said arithmetic operation circuit comprising: a first arithmetic operation section to perform a first arithmetic operation on said data by 32 bits using a generative polynomial; a second arithmetic operation section to perform a second arithmetic operation on said data by 32 bits using a generative polynomial; and a third arithmetic operation section to perform a third arithmetic operation on said data of 32 bits and on an arithmetic operation result of 32 bits being obtained at a midpoint in said first arithmetic operation section using said generative polynomial (col. 28, lines 13-32, Hyodo et al.).

Douady et al. teach a thirty-second order generative polynomial and a sixteenth order generative polynomial (col. 1, lines 59-64, Douady et al.).

- As per claim 23, Ishiwaki, Hyodo et al. and Douady et al. teach the additional limitations.

Ishiwaki teaches an arithmetic operation circuit for a cyclic redundancy check which performs arithmetic operations for error detection on data to be transmitted (col. 1, lines 8-11, Ishiwaki) using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished (col. 3, lines 49-50, Ishiwaki).

Hyodo et al. teach adding a result from each of said arithmetic operations to said data, said arithmetic operation circuit comprising: a first arithmetic operation section to perform a first arithmetic operation on said data by 32 bits using a generative polynomial; a second arithmetic operation section to perform a second arithmetic operation on said data by 32 bits using said generative polynomial; a third arithmetic operation section to perform a third arithmetic operation on said data of 32 bits and on a first arithmetic operation result of 16 bits being obtained at a midpoint in said first arithmetic operation section using said generative polynomial; a fourth arithmetic operation section to perform a fourth arithmetic operation on said data by 32 bits using said generative polynomial; and a fifth arithmetic operation section to perform a fifth arithmetic operation on said data of 32 bits, said first arithmetic operation result, and a second arithmetic operation result of 16 bits being obtained at a midpoint in said second arithmetic operation section using said generative polynomial (col. 28, lines 13-32, Hyodo et al.).

Douady et al. teach a sixteenth order generative polynomial (col. 1, lines 59-61, Douady et al.).

10. Claims 16, 18, 22, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiwaki (US 6,725,415 B2), Hyodo et al. (US 5,282,215) and Douady et al. (US 6,516,004 B1) as applied to claims 15, 17, 21, 23 above, and further in view of Henriksen (US 6,324,670 B1).

As per claim 16, Ishiwaki, Hyodo et al. and Douady et al. substantially teach the claimed invention described in claim 15 (as rejected above).

However Ishiwaki, Hyodo et al. and Douady et al. do not explicitly teach specifically that in said third arithmetic operation processing, said third arithmetic operation is performed by 64 bits in total by handling said data of 32 bits as low-order bits and said arithmetic operation result of 32 bits as high-order bits.

Henriksen in an analogous art teaches that register 406 is a 64-bit register and sections 408 and 410 are each 32-bits (figure 4, col. 6, lines 12-13, Henriksen).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ishiwaki's patent with the teachings of Henriksen by including additional that in said third arithmetic operation processing, said third arithmetic operation is performed by 64 bits in total by handling said data of 32 bits as low-order bits and said arithmetic operation result of 32 bits as high-order bits. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to simplify the circuit design for arithmetic processing of the bits for faster and accurate processing of the data.

- As per claim 18, Ishiwaki, Hyodo et al., Douady et al. and Henriksen teach the additional limitations.

Henriksen teaches that in the third arithmetic operation processing, the arithmetic operation is performed by 48 bits in total by handling said data of 32 bits as low-order bits and said first arithmetic operation result of 16 bits as high-order bits (col. 8, lines 55-56, Henriksen) and wherein, in said fifth arithmetic operation processing, said fifth arithmetic operation is performed by 64 bits in total by handling said data of 32 bits as low-order bits, said first arithmetic operation result of 16 bits as middle-order bits, and said second arithmetic operation result of 16 bits as high-order bits (col. 10, lines 27-30, Henriksen).

- As per claim 22, Ishiwaki, Hyodo et al., Douady et al. and Henriksen teach the additional limitations.

Henriksen teaches a data combining section to combine said data of 32 bits handled as low-order bits with said first arithmetic operation result of 32 bits handled as high-order and to feed combined results to said third arithmetic operation section (figure 4, figure 5A, 5B, col. 6, lines 12-13, col. 7, lines 20-24, Henriksen).

- As per claim 24, Ishiwaki, Hyodo et al., Douady et al. and Henriksen teach the additional limitations.

Henriksen teaches a first data combining section to combine said data of 32 bits with said first arithmetic operation result and to feed a combined result to said third arithmetic operation section, wherein as said combined result, said data of 32 bits is placed at low-order bits and said first arithmetic operation result is

placed at high-order bits, and a second data combining section to combine together said data of 32 bits, said first arithmetic operation result, and said second arithmetic operation result and to feed a combined result to said fifth arithmetic operation section, wherein as said combined result said data of 32 bits is placed at low-order bits and said first arithmetic operation result is placed at middle-order bits, and said second arithmetic operation result is placed at high-order bits (figure 5A, 5B, col. 7, lines 20-24, col. 8, lines 55-58, col. 10, lines 27-30, Henriksen).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100